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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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24504	7590	07/26/2007	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP			TAYLOR, BARRY W	
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STE 1750				
ATLANTA, GA 30339-5948			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,606	SEALS ET AL.	
	Examiner	Art Unit	
	Barry W. Taylor	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 06 May 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-12 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-12 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 18 February 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arvelo (7,082,107) in view of Tamura (2004/0248609).

Regarding claim 1. Arvelo teaches a method for output power dithering for improved transmitter performance (title, abstract), the method comprising:

transmitting a plurality of packets at a first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46) ;

determining a first error rate associated with the transmission of the plurality of packets at the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

transmitting the plurality of packets at least one second output power different from the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

determining at least one second error rate associated with the transmission at the at least one second output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46); and

identifying a desired output power based at least in part on a comparison between the first error rate and the at least one second error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

According to Applicants, Arvelo does not compare error rates to control output power (see paper dated 5/6/07, page 6).

Tamura also teaches power control by obtaining a difference between Block error rates (title, abstract, paragraphs 0003, 0005 – 0006, 0020 – 0024) so as to account for error rates that temporarily increase or decrease.

It would have been obvious for any one of ordinary skill in the art at the time of invention to modify the power control method and system as taught by Arvelo to obtain the difference between block error rates as taught by Tamura in order to prevent

unnecessary power increase caused in response to temporary quality degradation as disclosed by Tamura (paragraph 0022).

Regarding claim 2. Arvelo teaches a method for output power dithering for improved transmitter performance (title, abstract), the method comprising:

transmitting a plurality of packets at a first output power; determining a first error rate associated with the transmission of the plurality of packets at the first output power; transmitting the plurality of packets at a second output power if the first error rate is greater than a predetermined error rate value, wherein the second output power is different from the first output power; determining a second error rate associated with the transmission at the second output power; and adjusting the second output power if the second error rate is lower than the first error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

According to Applicants, Arvelo does not compare error rates to control output power (see paper dated 5/6/07, page 6).

Tamura also teaches power control by obtaining a difference between Block error rates (title, abstract, paragraphs 0003, 0005 – 0006, 0020 – 0024) so as to account for error rates that temporarily increase or decrease.

It would have been obvious for any one of ordinary skill in the art at the time of invention to modify the power control method and system as taught by Arvelo to obtain the difference between block error rates as taught by Tamura in order to prevent unnecessary power increase caused in response to temporary quality degradation as disclosed by Tamura (paragraph 0022).

Regarding claim 3. Arvelo teaches where the second output power is adjusted until a desired value of the second error rate is reached (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

Regarding claim 4. Arvelo teaches transmitting the plurality of packets at a third output power if the second error rate is not lower than the first error rate, wherein the third output power is different from the first output power and the second output power; determining a third error rate associated with the transmission at the third output power; and adjusting the third output power if the third error rate is lower than the first error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

Regarding claim 5. Arvelo teaches transmitting the plurality of packets at the first output power if the third error rate is not lower than the first error rate (col. 4 lines 43-50).

Regarding claim 6. Arvelo teaches resuming transmission of the plurality of packets at the first output power if the first error rate or the second error rate is not determined based on a predetermined criterion (col. 4 lines 43-50).

Regarding claim 7. Arvelo teaches the first error rate and the second error rate are determined based on a number of failed acknowledgements of transmitted packets (col. 5 lines 21-50).

Regarding claim 8. Arvelo teaches transmission at the first output power and second output power is associated with a variable data rate (title, abstract, col. 3 lines 12-13).

Regarding claim 9. Arvelo teaches wherein the first error rate, the second error rate and the predetermined error rate value are associated with the variable data rate (title, abstract, col. 3 lines 12-13).

Regarding claim 10. Arvelo teaches a system for output power dithering for improved transmitter performance (title, abstract), the system comprising:

a transmitter that transmits a plurality of packets at a first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46); and

a processor that determines a first error rate associated with the transmission of the plurality of packets at the first output power;

causes the transmitter to transmit the plurality of packets at least one second output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

determines at least one second error rate associated with the transmission at the at least one second output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46); and

identifies a desired output power based at least in part on a comparison between the first error rate and the at least one second error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

According to Applicants, Arvelo does not compare error rates to control output power (see paper dated 5/6/07, page 6).

Tamura also teaches power control by obtaining a difference between Block error rates (title, abstract, paragraphs 0003, 0005 – 0006, 0020 – 0024) so as to account for error rates that temporarily increase or decrease.

It would have been obvious for any one of ordinary skill in the art at the time of invention to modify the power control method and system as taught by Arvelo to obtain the difference between block error rates as taught by Tamura in order to prevent unnecessary power increase caused in response to temporary quality degradation as disclosed by Tamura (paragraph 0022).

Regarding claim 11. Arvelo teaches a system for output power dithering for improved transmitter performance (title, abstract), the system comprising:

means for transmitting a plurality of packets at a first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

means for determining a first error rate associated with the transmission of the plurality of packets at the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

means for transmitting the plurality of packets at least one second output power different from the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

means for determining at least one second error rate associated with the transmission at the at least one second output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46); and

means for identifying a desired output power based at least in part on a comparison between the first error rate and the at least one second error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

According to Applicants, Arvelo does not compare error rates to control output power (see paper dated 5/6/07, page 6).

Tamura also teaches power control by obtaining a difference between Block error rates (title, abstract, paragraphs 0003, 0005 – 0006, 0020 – 0024) so as to account for error rates that temporarily increase or decrease.

It would have been obvious for any one of ordinary skill in the art at the time of invention to modify the power control method and system as taught by Arvelo to obtain the difference between block error rates as taught by Tamura in order to prevent unnecessary power increase caused in response to temporary quality degradation as disclosed by Tamura (paragraph 0022).

Regarding claim 12. Arvelo teaches a computer readable medium having code for causing a processor to perform output power dithering for improved transmitter performance (title, abstract, col. 9 lines 38-46), the computer readable medium comprising:

code adapted to transmit a plurality of packets at a first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

code adapted to determine a first error rate associated with the transmission of the plurality of packets at the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

code adapted to transmit the plurality of packets at least one second output power different from the first output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46);

code adapted to determine at least one second error rate associated with the transmission at the at least one second output power (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46); and

code adapted to identify a desired output power based at least in part on a comparison between the first error rate and the at least one second error rate (title, abstract, figures 1 and 3, col. 3 lines 12-33, col. 3 line 63 – col. 4 line 65, col. 5 lines 21-61, col. 10 lines 37-46).

According to Applicants, Arvelo does not compare error rates to control output power (see paper dated 5/6/07, page 6).

Tamura also teaches power control by obtaining a difference between Block error rates (title, abstract, paragraphs 0003, 0005 – 0006, 0020 – 0024) so as to account for error rates that temporarily increase or decrease.

It would have been obvious for any one of ordinary skill in the art at the time of invention to modify the power control method and system as taught by Arvelo to obtain the difference between block error rates as taught by Tamura in order to prevent

unnecessary power increase caused in response to temporary quality degradation as disclosed by Tamura (paragraph 0022).

Response to Arguments

2. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry W. Taylor, telephone number (571) 272-7509, who is available Monday-Thursday, 6:30am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost, can be reached at (571) 272-7872. The central facsimile phone number for this group is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group 2600 receptionist whose telephone number is (571) 272-2600, the 2600 Customer Service telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Barry W. Taylor
Art Unit 2617

Barry W. Taylor 7/11/07
BARRY TAYLOR
PRIMARY EXAMINER